

MT60G008CN5

N-Channel Enhancement Mode Power MOSFET



MT Semiconductor®

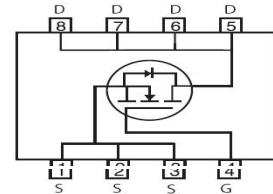
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V_{DS}	60	V
$R_{DS(on),TYP@ V_{GS}=10V}$	0.9	mΩ
$I_D(\text{Silicon limited})$	370	A

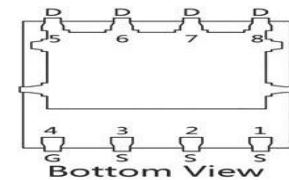
Features

- Enhancement mode
- Ultra low $R_{DS(on)}$ to minimize conduction losses
- 100% Avalanche tested, 100% R_g tested
- Optimized Q_g , Q_{gd} , and Q_{gd}/Q_{gs} ratio to minimize switching losses

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$ 291	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$ 370	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$ 234	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 1150	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$ 35	A
		$T_A = 70^\circ\text{C}$ 28	A
E_{AS}	Avalanche energy, single pulsed ②	1225	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$ 291	W
		$T_C = 100^\circ\text{C}$ 116	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$ 2.6	W
		$T_A = 70^\circ\text{C}$ 1.7	W
T_J, T_{STG}	Operating junction and storage temperature range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.36	0.43	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	40	48	$^\circ\text{C}/\text{W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250μA	60	--	--	V
I _{DSS}	Zero gate voltage drain current(T _j =25°C)	V _{DS} =60V, V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _j =125°C) ^⑦	V _{DS} =60V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-body leakage current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250μA	2.5	3.0	3.5	V
R _{DS(on)}	Drain-source on-state resistance ^⑧	V _{GS} =10V, I _D =40A	--	0.9	1.2	mΩ
		(T _j =100°C) ^⑦	--	1.3	--	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	94	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ^⑦	V _{DS} =30V, V _{GS} =0V, f=100kHz	--	6235	--	pF
C _{oss}	Output capacitance ^⑦		--	1635	--	pF
C _{rss}	Reverse transfer capacitance ^⑦		--	75	--	pF
R _g	Gate resistance	f=1MHz	--	2.1	--	Ω
Q _g	Total gate charge ^⑦	V _{DS} =30V, I _D =40A, V _{GS} =10V	--	98	--	nC
Q _{gs}	Gate-source charge ^⑦		--	32	--	nC
Q _{gd}	Gate-drain charge ^⑦		--	24	--	nC
Switching Characteristics ^⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =30V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	20	--	ns
T _r	Turn-on rise time		--	72	--	ns
T _{d(off)}	Turn-off delay time		--	59	--	ns
T _f	Turn-off fall time		--	36	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.78	1	V
T _{rr}	Reverse recovery time ^⑦	V _{DD} =30V, I _{sd} =40A, V _{GS} =0V	--	63	--	ns
Q _{rr}	Reverse recovery charge ^⑦	di/dt=100A/μs	--	73	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This value is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 70A, V_{GS} = 10V; 100% FT tested at L = 0.1mH, I_{AS} = 65A.
- ③ The power dissipation P_d is based on T_{j(max)}, using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_{j(max)}, using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

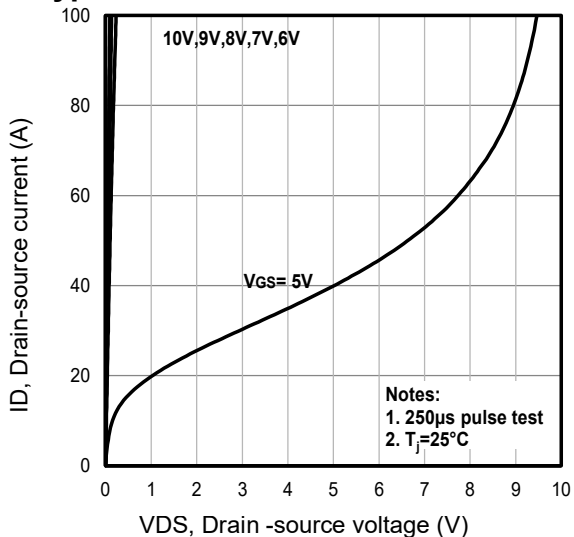


Fig1. Typical output characteristics

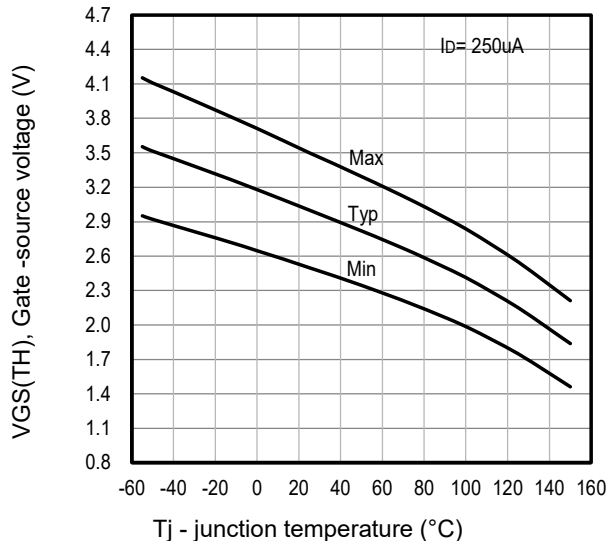


Fig2. Typical VGS(TH) gate-source voltage Vs. Tj

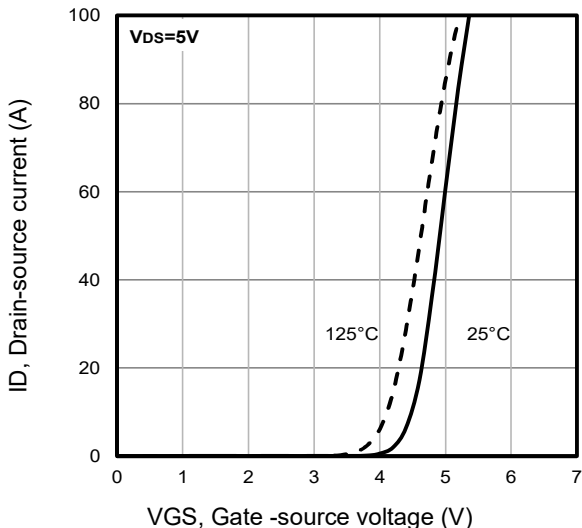


Fig3. Typical transfer characteristics

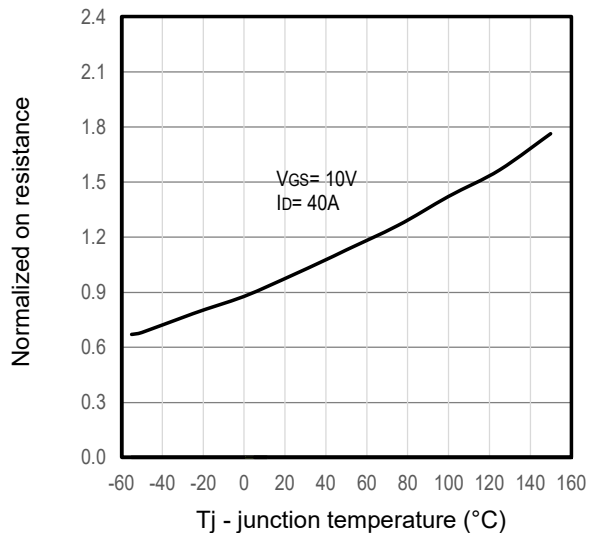


Fig4. Typical normalized on-resistance Vs. Tj

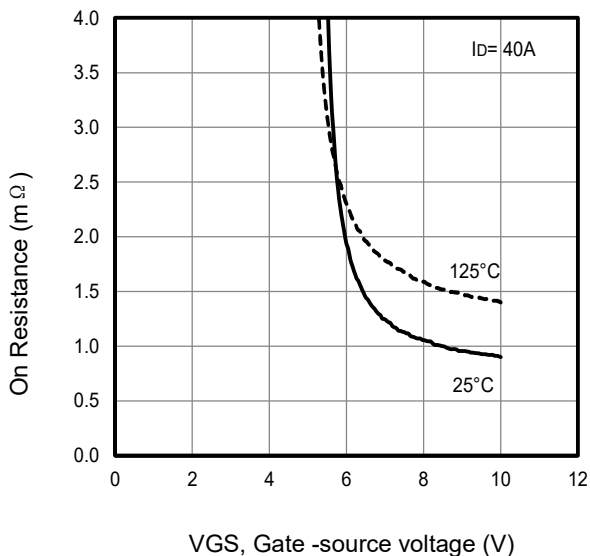


Fig5. Typical on resistance Vs gate-source voltage

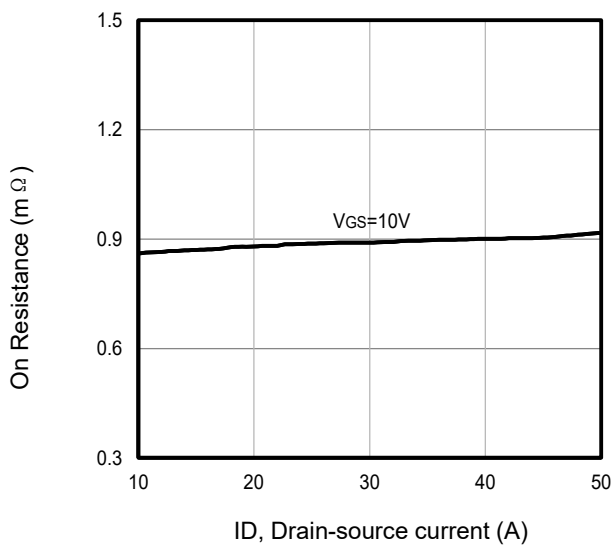


Fig6. Typical on resistance Vs drain current

Typical Characteristics

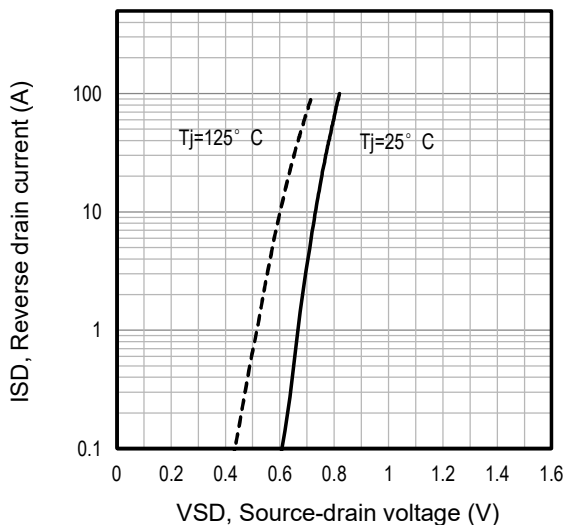


Fig7. Typical source-drain diode forward voltage

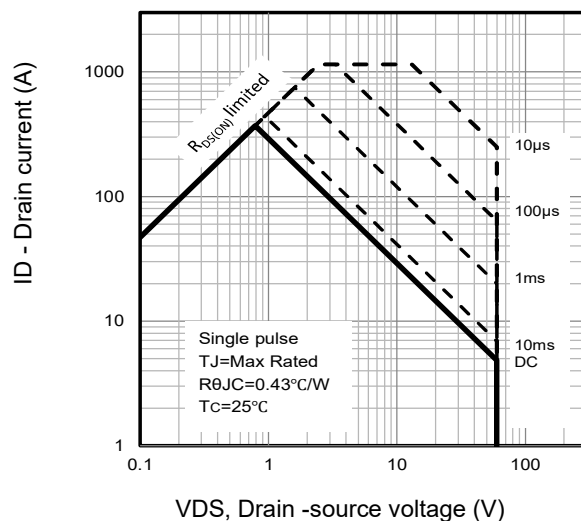


Fig8. Maximum safe operating area

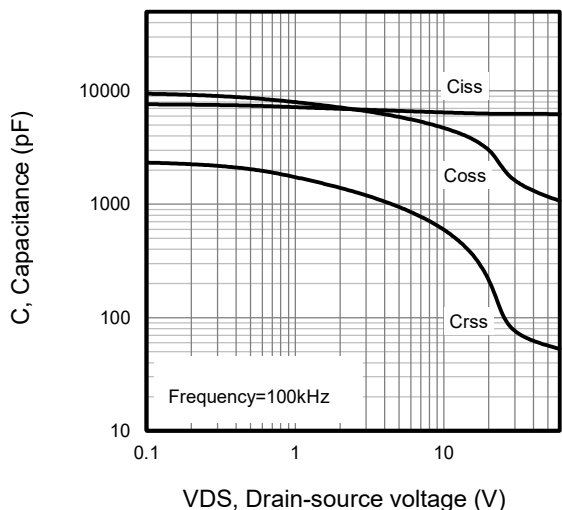


Fig9. Typical capacitance Vs. drain-source voltage

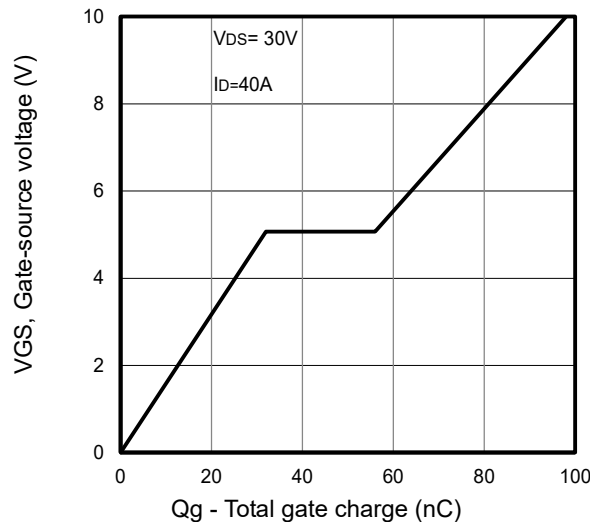


Fig10. Typical gate charge Vs. gate-source voltage

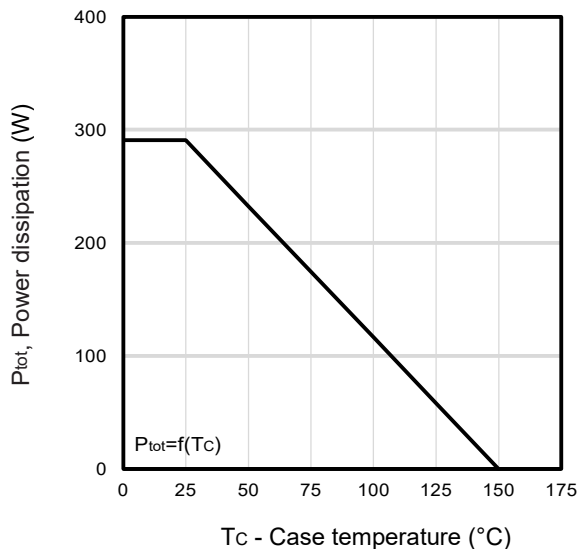


Fig11. Power dissipation Vs. case temperature

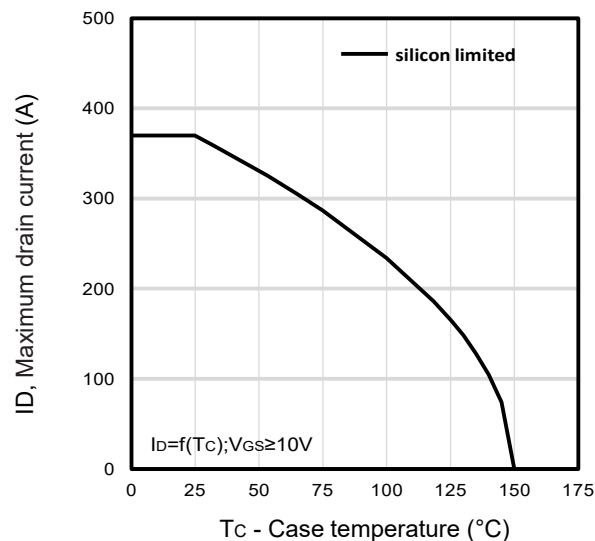


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

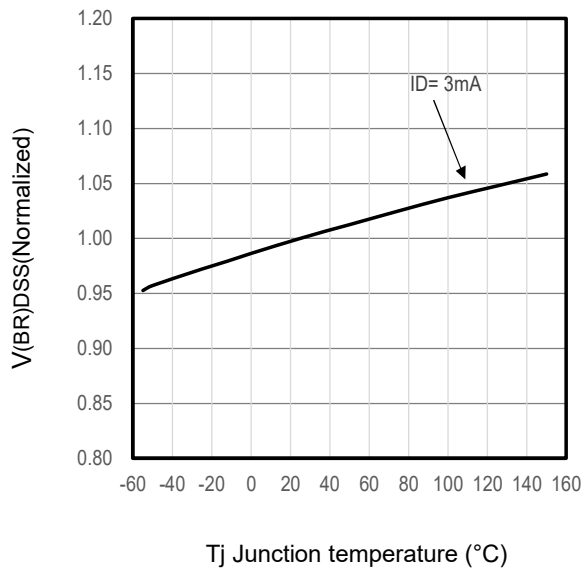


Fig13. Typical V(BR)DSS Vs Tj

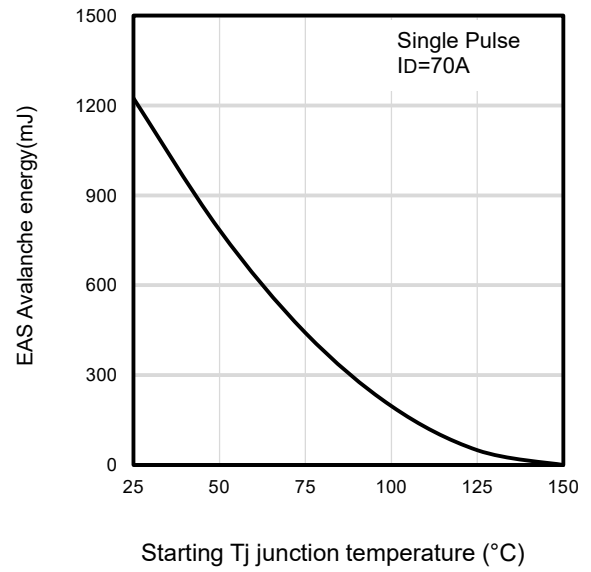


Fig14. Maximum avalanche energy vs temperature (°C)

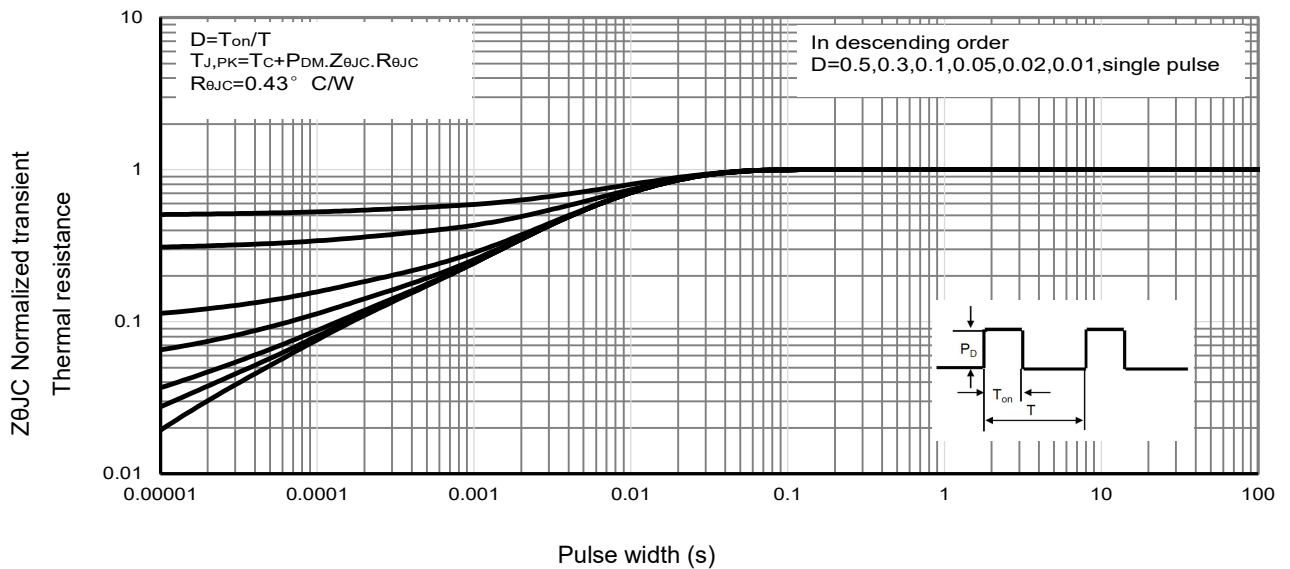


Fig15 . Normalized maximum transient thermal impedance

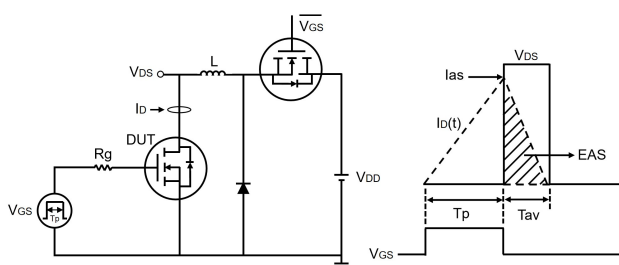


Fig16. Unclamped Inductive Test Circuit and waveforms

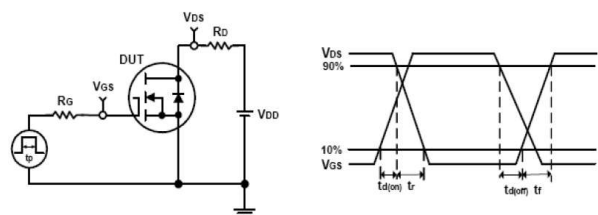
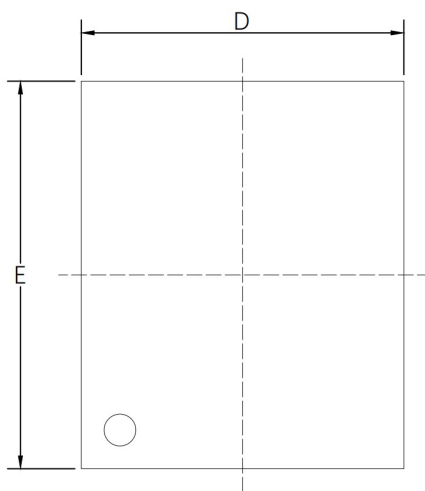


Fig17. Switching Time Test Circuit and waveforms

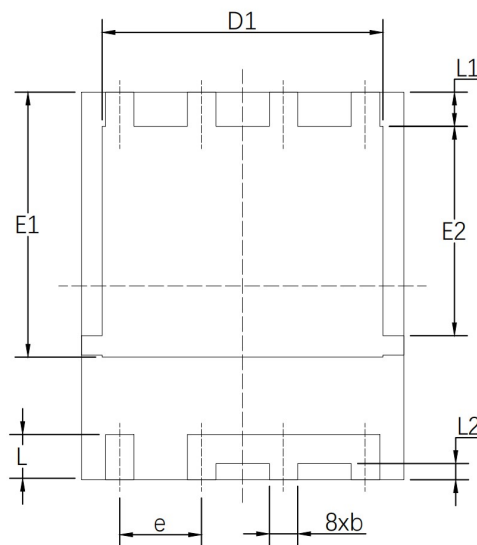
TDFN5x6FL Package Outline Data



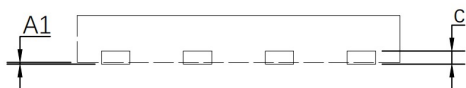
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
b	0.34	0.44	0.54
c	0.203 REF.		
D	4.90	5.00	5.10
D1	4.25	4.35	4.45
E	5.90	6.00	6.10
E1	4.00	4.10	4.20
E2	3.14	3.24	3.34
e	1.27 BSC		
L	0.60	0.70	0.80
L1	0.43	0.53	0.63
L2	0.25 REF.		

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